International Journal of Research in Social Sciences Vol. 9 Issue 3, March 2019, ISSN: 2249-2496 Impact Factor: 7.081 Journal Homepage: http://www.ijmra.us, Email: editorijmie@gmail.com Double-Blind Peer Reviewed Refereed Open Access International Journal - Included in the International Serial

Directories Indexed & Listed at: Ulrich's Periodicals Directory ©, U.S.A., Open J-Gage as well as in Cabell's Directories of Publishing Opportunities, U.S.A

DESIGN OF LOW POWER ALU USING FINFETS

Susmita Mahan^{*}

Raghvendra Singh**

Abstract: We are moving towards the era of minimization of transistor size, short channel effects (SCE) are becoming major concern. Double gate FinFETs are emerging transistors, which gives better SCEs performance compared to conventional Mosfet transistors. Adder and sub-tractors are basic component in computation. Most of the operation multiplication, division, ripple carry addition etc. A 1-bit ALU has been designed using MOSFET and FinFET and simulated, which implements four basic operations like addition, subtraction, AND,OR. All the results are carried out using H-spice simulation tool. The simulation of ALU is carried at 32nm technology. The results obtained from simulation of FinFET ALU are compared with conventional MOS ALU. The figure of merit measured for ALU are power and delay.

KEYWORDS- FinFET, CMOS, Short channel effects (SCEs), Circuit Design, Device simulation, ALU, H-spice.

^{*} M.Tech. Scholar, EC Department, faculty of Engineering & Technology, Mandhana Kanpur, Uttar Pradesh, India

^{**} Assistant professor in department, electronic & communication engineering, Faculty of Engineering & Technology, Rama University, Kanpur, India

Introduction: In 1947, there was the point-contact transistor. This was the very first transistor ever made, built by Walter Brattain with the help of John Bardeen. It was made of two gold foil contacts sitting on a germanium crystal. In 1951, the first big change in transistors occurred when William Shockley developed a junction transistor. The first junction transistors were sandwiches of N- and P-type germanium (germanium with an excess and scarcity of electrons, respectively). A weak voltage coming into the middle layer would affect another current traveling across the entire sandwich. The next big jump in transistor evolution came with the field-effect transistor in 1960's. Most modern transistors are field-effect transistors -- specifically metal-oxide semiconductor field-effect transistors, or "MOSFETs." Instead of being a sandwich, MOSFETs have a channel of either N- or P- type semiconductor running through a ridge on top of the other type. The working principle of MOSFET depends up on the MOS capacitor. The MOS capacitor is the main part. The semiconductor surface at below the oxide layer.

4 FinFET Technology

Finfet in classified as a type of a magnitude metal oxide semiconductor field effect transistor. It was developed at the university of Berkley California by Chenning Hu and his colleagues.

In FinFET the NMOS in CMOS technology is replaced with N-Finfet and PMOS with P-Finfet ,both gates of Finfet are together [3] BY using we can design a Finfet version of a CMOS logic circuit or pass transistor logic circuit that retains the same functionalities as the MOSFET version.[1] in the Finfet provides better circuit performance and reduces leakage current through effective suppression of short channel effect and near ideal sub threshold swing [2].

In the single gate mode the short channel effects are less server than those of the device in the double gate mode[2].

Arithmetic Logic Unit

An arithmetic logic unit (ALU) is a digital circuit used to perform arithmetic and logic operations. It represents the fundamental building block of the central processing unit (CPU) of a computer. Modern CPUs contain very powerfuland complex ALUs. In addition to ALUs, modern CPUs contain a control unit (CU). Most of the operations of a CPU are performed by one or more ALUs, which load data from input registers. A register is a small amount of storage available as part of a CPU. The control unit tells the ALU what operation to perform on that data

and the ALU stores the result in an output register. The control unit moves the data between these registers, the ALU, and memory.

PRAPOSED AIRTHMETICE LOGIC UNIT DESIGN USING FINFETS

Arithmetic and logical unit is a combinational logic unit that performs its arithmetic and logical operations. The design of 1 bit ALU which perform two arithmetic and two logical operations. The two arithmetic operations includessingle-bit addition and subtraction operations. The two logical operation includes single-bit AND and OR operations. The output of four operations goes to 4:1 multiplexer which select one of results according to the status of select lines and gives output. The block diagram of 1-bit ALU is shown below in Figure 1.

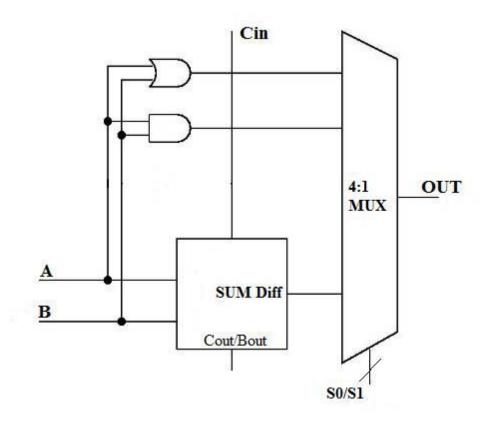


Figure1: 1-bit Block Diagram of ALU

The logic circuits of AND, OR, Inverter, full Adder and multiplexer are made using CMOS logic replacing the conventional MOSFETs with FinFETs

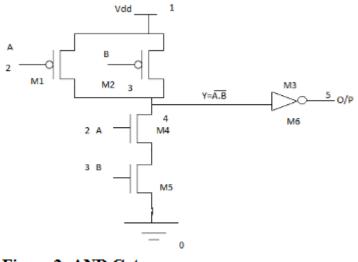


Figure 2: AND Gate

Figure 1 shows the block diagram of Airthmetic logic unit , and the CMOS circuit with nodes of AND OR and Full adder are shoen the fifure 2,3,4 respectively.

OR GATE

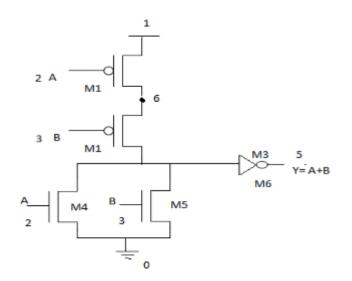


Figure-3

The transistor symbols used in figure of a MosFET, FinFET symbols as studied [3] is show in figure 5. ALL the circuits are made in short gate configuration of FinFET as show in the figure 5.

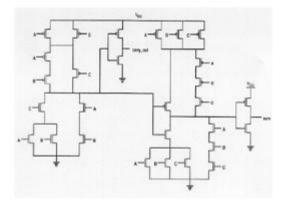
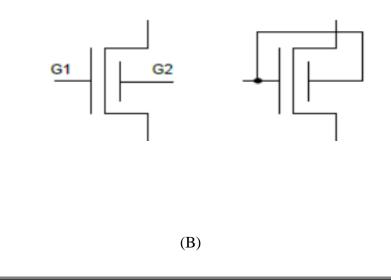


Figure 4 : Full Adder

The ciruit diagram nodes are given different node name for which the FinFET model from BSIMCMG is included and simulated. The 2-bit opcode selects the result of either logical or arithmetic block which will be the output of the ALU.



544

Figure 5: FinFET configuration (a) Independent Gates(b)Shorted Gates

RESULT AND SIMULATION

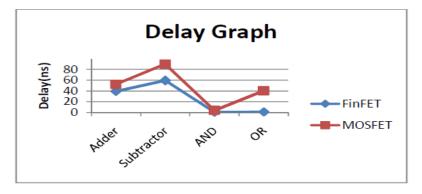
1.DELAY AND POWER CALCULATION

The delay is calculated as the time difference between 50% of rise in input to 50% of rise in output. The fall delay is calculated by the time difference between the 50% of fall in input to 50% fall in the output. The delay of sub blocks is given in Table 1.1, below which show the results for delay in both FinFET and MOSFET.

Operation	FinFET	MOSFET	
Addition	39.18ns	50.5ns	
Subtraction	59.28ns	88.60ns	
AND	0.15ns	3.7ns	
OR	0.98ns	40.1ns	

Table1. 1:Delay Of ALU Design Operations

In the Figure 5.1, it shows the delay graph between MOSFET and FinFET it shows the variations in delay for each sub block in FinFET is better than MOSFET.





Average power calculated for FinFET is less than MOSFET. Table 1.2, below show the average power of the sub blocks using MOSFET and FinFET.

Operations	FinFET	MOSFET	
Addition	0.040nw	24.44uw	
Subtraction	0.095nw	19.5uw	
AND	0.096pw	3.61ue	
OR	0.10pw	1.24uw	

Table1. 2 : Power of ALU Design Operation

In the Figure 5.2, it shows that the average power variations between MOSFET and FinFET for each sub-block of ALU and also shows that average power in FinFET is less than MOSFET

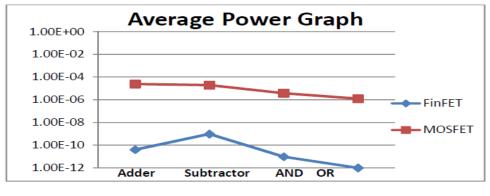


Figure 5.2 : Average Power analysis of MOSFET FinFET

From both the architectures the average power and delay has been calculated below in table 1.3, From this Table it is observed that delay and average power consumed by FinFET is far less than the delay and power consumed by MOSFET which results that the FinFET have faster speed less power dissipation than the MOSFET.

	Delay	Power
FinFET	4.45ns	23uw
MOSFET	67.1ns	0.317mw

Table1. 3 :Comparison between Power and Delay of FinFET and MOSFET

REFERENCES

1. Mahender Veshala, IJEIT 2013, "Reduction of short-channel effects in FinFET".

2. Tushar Surwadekar. IJETT-2014, "Deep submicron 50nm CMOS logic design with FinFETs".

3. V Narendar, IJCA 2012, "Design of high performance Digital logic circuits basedon Finfet technology".

4. Zhichao Lu, IEEE, vol 28, feb-2007, "short channels effects in FinFET".

5. Pc Rajshree, ICIET 2014, "Deep submicron 50nm CMOS logic design with Finfet".

6. Sherif A.Tawfika, Elsevier, "2011, Finfet domino logic with independent gate keepers".

7. S.Jim Hawkinson, "Analysis and performance comparision of CMOS and Finfet for VLSI application" IJET and advance Engineering Volume 3, issue2 feb 2013.

8. Anthony Chand , " Cost affective ALU designs that save energy with increased performance".Department of electrical and computer engineering. University of Central Florida.

9. Michael C. Wang, "Independent gate FinFET circuit design methodology." IAENG international journal of computer science, 37:1, IJCS_37_1_06

10. Prateek Mishra, Ansh Muttreja, and Niraj k. Jha, "FinFET circuit design". Springer Science business media,LLC 2011.

11. Sameer Dwivedi, Dr, Neelam Rup Prakash. " A study on recent advancements in VLSI Technology using FinFET".International Journal of innovative Research in science, Engineering and Technology, Vol 4,Issue 12 Dec 2015.